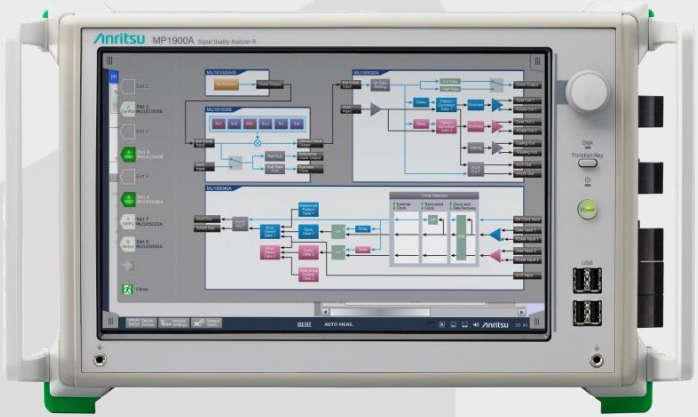
Anritsu envision : ensure

Signal Integrity Analysis
Multi-channel High-Performance BERT

Signal Quality Analyzer-R
MP1900A Series

SQA-R



Outline

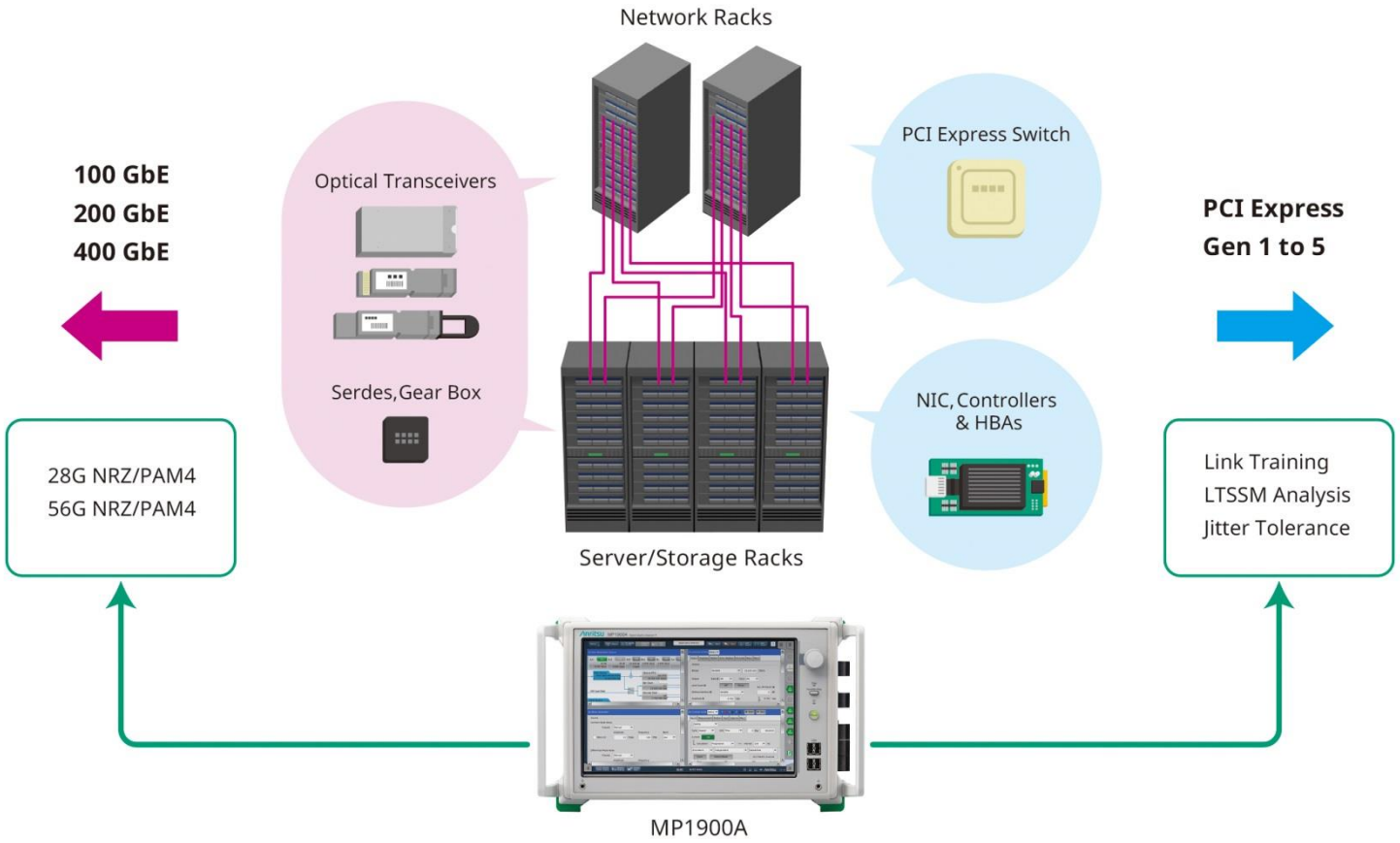
- Due to the explosive growth of data traffic resulting from the popularity of smartphones and mobile terminals, data centers are transitioning network interfaces to faster 200/400 GbE standards, and PCI bus interconnects speeds now exceed 10G. In addition, support for multi-channels is also increasing transitioning.
- The Signal Quality Analyzer-R MP1900A series is an 8-slot modular type, high-performance BERT with excellent expandability supporting measurement applications by installing 32 Gbit/s Multi-channel PPG, ED, and Jitter/Noise addition modules for signal integrity analysis of increasingly faster devices. Moreover, as well as functions for evaluating the Physical layer of high-speed interfaces, the built in Link Training/LTSSM analysis function supports all in one measurement of high-speed network interfaces such as 200/400 GbE, and bus interfaces such as PCIe.

MP1900A Series Supported Applications

100 GbE/200 GbE/400 GbE, CEI-25G/28G/56G/112G, InfiniBand EDR/HDR, Fibre Channel
PCI Express Gen1 to 5, Thunderbolt 3, USB3.1 Gen1/2
Optical Module, SERDES, AOC, High-Speed Interconnect

MP1900A Update Points

The MP1900A series is a high-expandability, high-performance BERT supporting physical layer evaluations of high-speed interfaces. The all-in-one design covers early stage R&D evaluations ranging from next-generation 200/400 GbE network interfaces to PCI Express, etc., bus interfaces.



MP1900A Series Features

Excellent expandability

- 8 slots (per one MP1900A main unit)
- Maximum transmission capacity up to 512 Gbit/s supporting up to 16ch of NRZ (using 2ch PPG in all 8 slots)
- All-in-one support for both high-speed network interfaces and bus interfaces such as PCIe

Full support for high-speed device signal integrity evaluations

- Bit rates of 2.4 Gbit/s to 32.1 Gbit/s
- 10Tap Emphasis
- Multi-band CTLE (supports 8, 16, and 28 Gbit/s bands)
- Low Intrinsic Jitter data output 115 fs rms (typ.)
- High input sensitivity 15 mV (Eye Height) (typ.)
- NRZ/PAM4 support
- CDR SSC support
- Jitter (SJ/RJ/BUJ/SSC) and noise (CM/DM/White) tolerance measurements

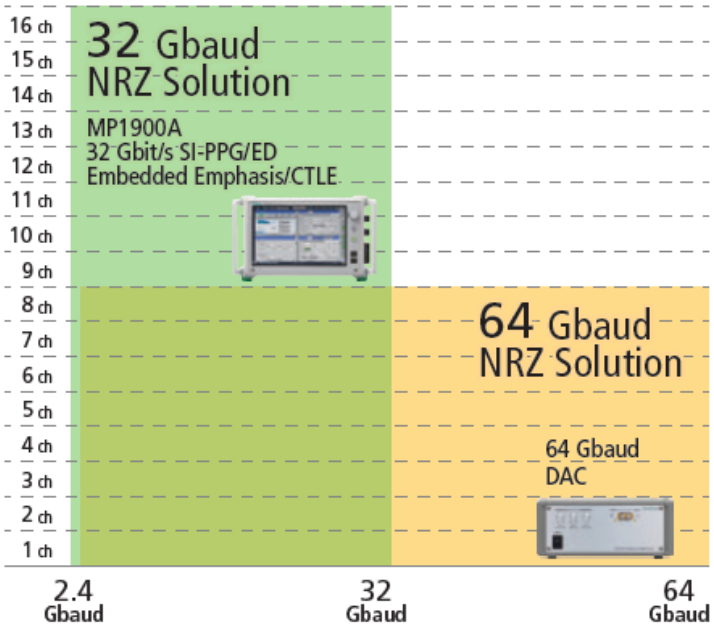
Support for PCIe receiver tests

- Supports PCIe Gen1 to Gen4 as well as future Gen5 with no hardware upgrades
- Protocol Aware
- Link Negotiation and LTSSM analysis functions

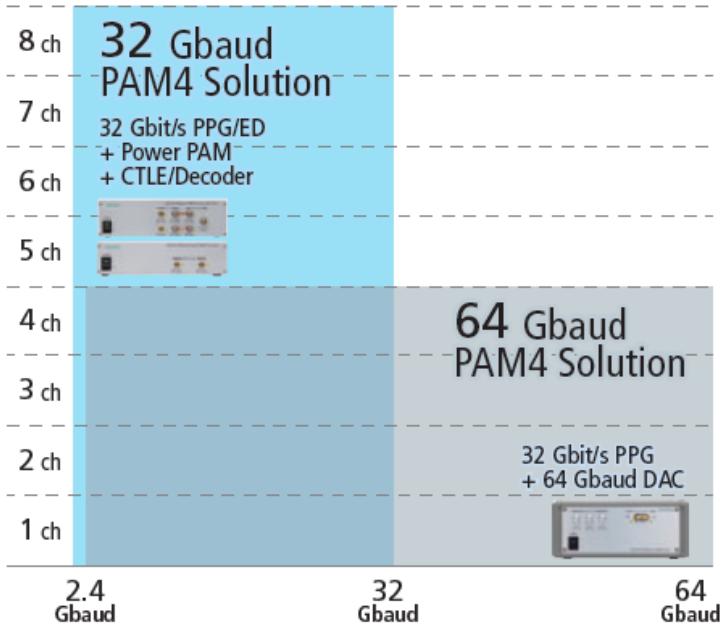
Supports Wideband & Multi-channel Measurement Requirements

The 8-slot modular type Signal Quality Analyzer-R MP1900A can be easily customized to support more measurement channels. In addition, adding a remote-box expansion, such as the PAM4 converter and 64G MUX/DEMUX, offers new required functions and performance without wasting previous capital equipment costs. With cost-effective upgrade support for next-generation interfaces, such as 400 GbE, the MP1900A will play a key role in bringing customers' products more quickly to market .

Multi-channel NRZ solutions



Multi-channel PAM4 solutions

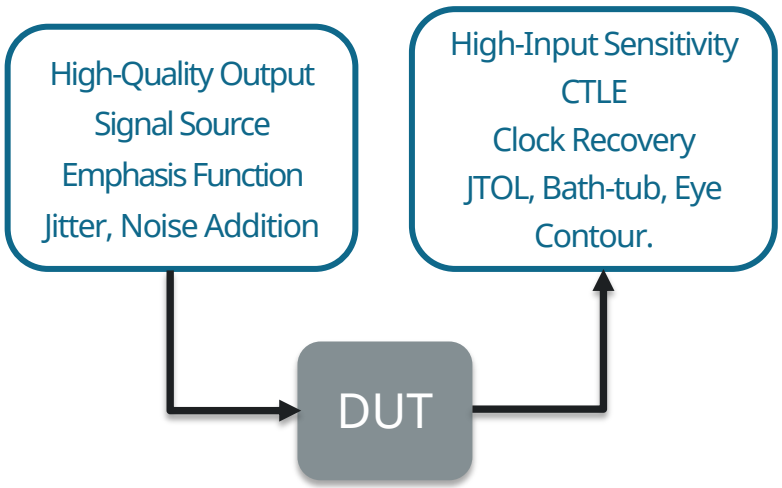


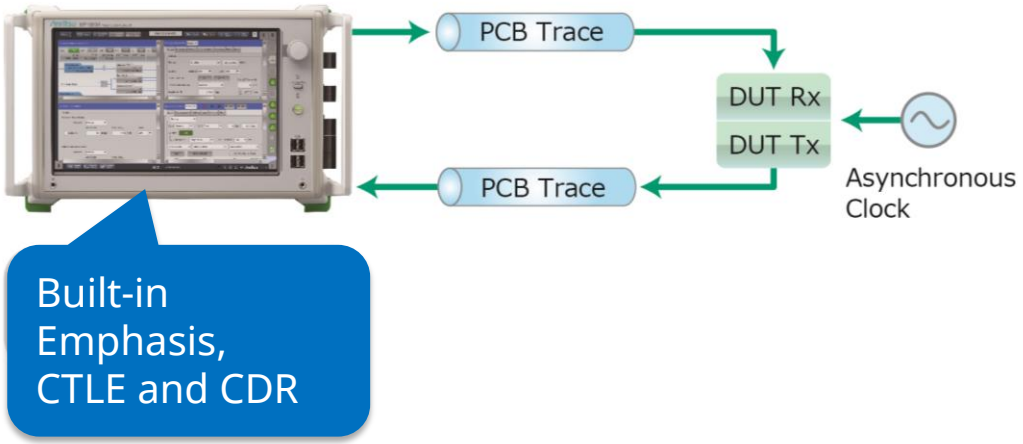
Ideal for Signal Integrity Evaluations (1/2)

The 21G/32G bit/s SI PPG MU195020A has a built in 10Tap (max.) Emphasis option for simulating various devices and channels as well as for outputting corrected waveforms reproducing channel-path losses to help improve design evaluation efficiency.

The Rx-side 21G/32G bit/s SI ED MU195040A has a built in multi-band CTLE (Continuous Time Linear Equalization) function supporting 28, 16, and 8 Gbit/s band input signals for performing BER measurements of Eyes closed by transmission path losses. Since this CTLE function is a hardware equalizer rather than software emulator, it supports evaluation of TRx BER performance under near-to-live conditions, such as BER evaluation of test signals, and comparison of DUT BER measurement results.

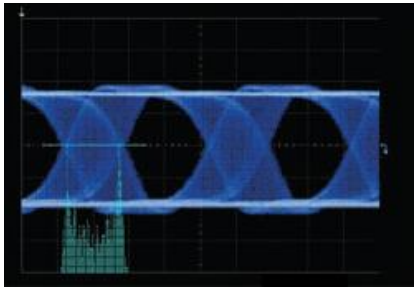
Signal Integrity Evaluations
Required Performance and Functions



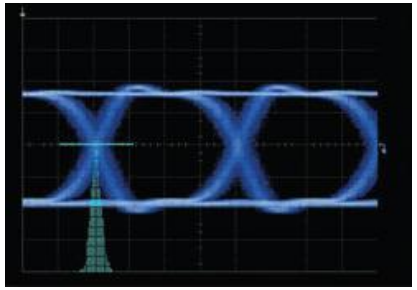


Ideal for Signal Integrity Evaluations (2/2)

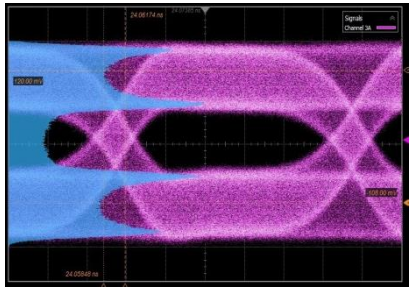
To perform high-speed receiver stressed input tolerance tests, the BER is measured under the worst conditions using a stressed signal with added jitter and voltage noise. Using the MP1900A series with the Jitter Modulation Source MU181500B, Noise Generator MU195040A with CDR function for adding various Jitter types and SSC and the Jitter Tolerance Test MX183000A-PL001 software, supports receiver tolerance tests in conformance with the various interface standards. The MP1900A series offers strong support for receiver stressed input tolerance tests by high-quality output signal before jitter and noise addition and high-linearity jitter and noise addition functions.



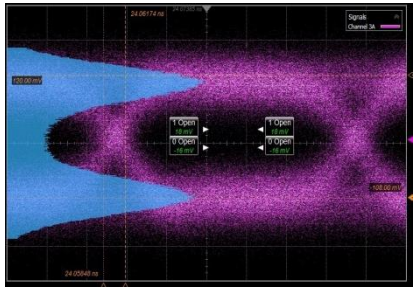
Sinusoidal Jitter(SJ)



Random Jitter(RJ)



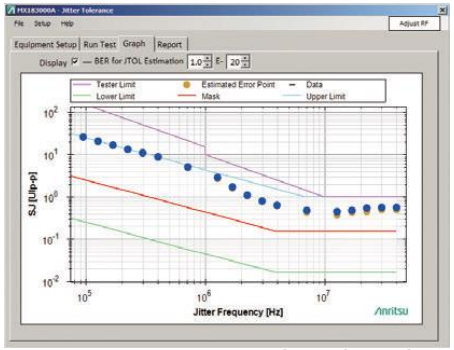
CM/DM Noise



White Noise

Jitter Tolerance Test Function (MX183000A-PL001)

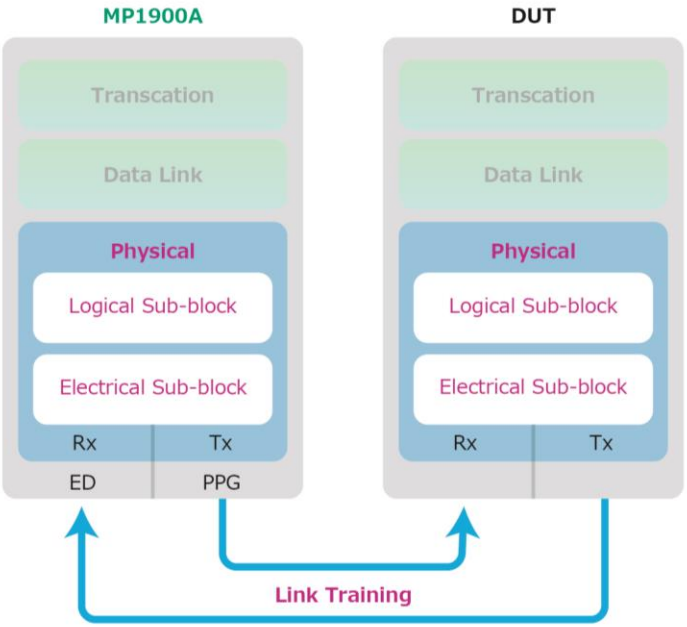
- High-versatility Jitter Tolerance measurements
- PHY Device Jitter Tolerance tests by impressing SJ/RJ/BUJ
- Standards-compliant Mask measurements
- Fast measurement times using low error rate estimation function, such as 1E–12 and 1E–15
- Tolerance measurements versus device characteristics using four Binary, Upward, Downward, Binary + Linear methods



Low Error Rate Estimation Jitter Tolerance Measurements

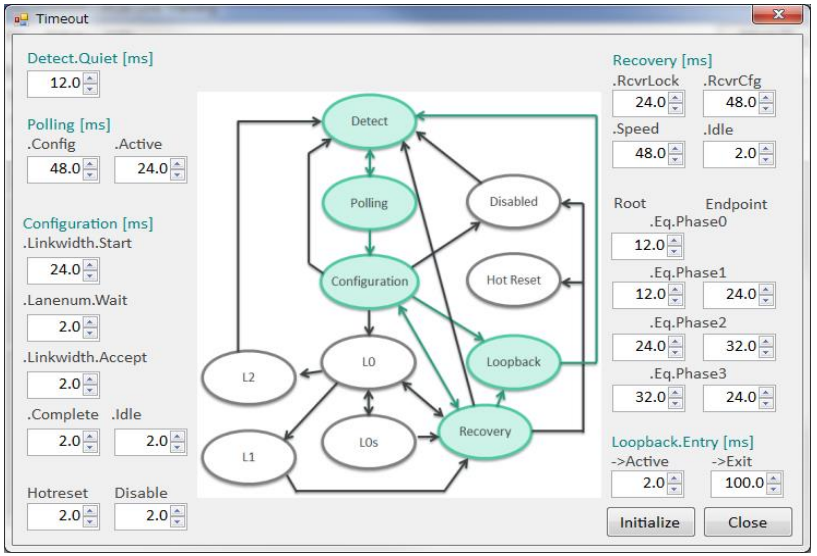
Built-in PCI Express Link Training and LTSSM Analysis Functions

High-speed serial interfaces require good interconnectivity between devices and equipment, and it is important to identify whether a dropped Link is caused by physical or logical errors. The all-in-one MP1900A series supports Physical layer evaluations for PCIe Gen1 to Gen4 and future Gen5 receivers, in addition to having Link Training for securing normal operation, also has functions for detecting and analyzing LTSSM (Link Training Status State Machine) fault transitions to improve detection efficiency.



Supports physical layer measurements of add-in cards and system boards

- Tx/Rx Link Equalization Response Test
- Rx Link Equalization Test
- Receiver Jitter Tolerance Test



PCI Express Link Training State transitions (MX183000A-PL021)

New Features of MP1900A Series

- 8-slot Platform
- 32G SI PPG/ED and Noise Generator Modules
- PCI Express Link Training and LTSSM Analysis Functions
- Backward Compatibility with SQA Series MU181000B Synthesizer, Jitter Modulation Source MU181500B, and 32G PPG/ED MU183020A/40B*

Signal Quality Analyzer-R MP1900A

MX183000A-PL021
PCIe Link Training
(software)

21G/32G bit/s SI PPG MU195020A

21G/32G bit/s SI ED MU195040A

Noise Generator MU195050A

*Future support for the 32G 4ch PPG/ED series MU183021A/41B is expected. Refer to the selection guides for details.

21G/32G bit/s SI PPG MU195020A Features

- Bit rate of 2.4 to 21 Gbit/s or 32.1 Gbit/s
- 1ch/2ch Selection
- 10Tap Emphasis built-in
- Data Output Amplitude 0.1 Vp-p to 1.3 Vp-p (Single-end)
  0.2 Vp-p to 2.6 Vp-p (Differential)
- Low Intrinsic Jitter output of 115 fs rms (typ.)
- Tr/Tf (20%-80%) of 12 ps (typ.)
- Multi-channel synchronization function
- NRZ/PAM4 support (PAM4 uses 2ch Data out + G0375A remote head)
- PCI Express Link Training

21G/32G bit/s SI PPG MU195020A

Data1 (differential) **Data2 (differential)**

・10Tap Emphasis
・High-Quality Output Waveforms
・Multi-channel Synchronization

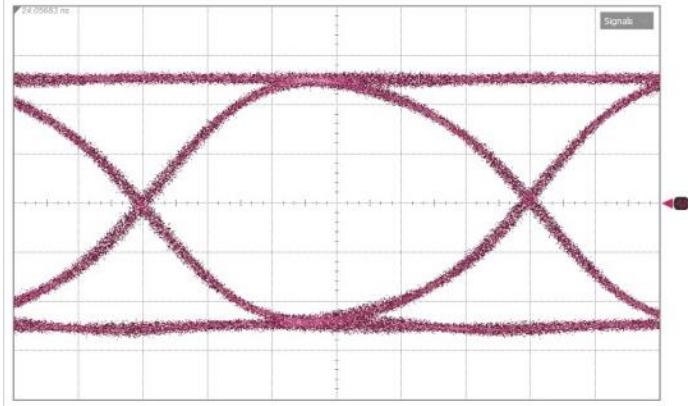
DUT

MU195020A PPG Data Output Waveforms

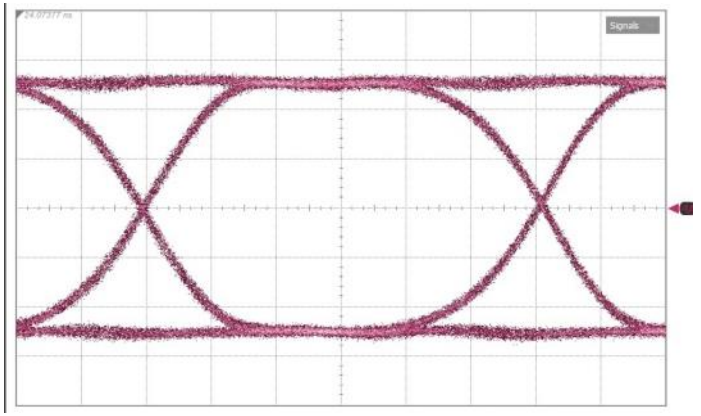
Low Intrinsic Jitter Data Output Waveforms for Signal Integrity Analysis

PRBS 2^{31}-1, 1 Vp-p (Single end, 70 GHz observed with oscilloscope)

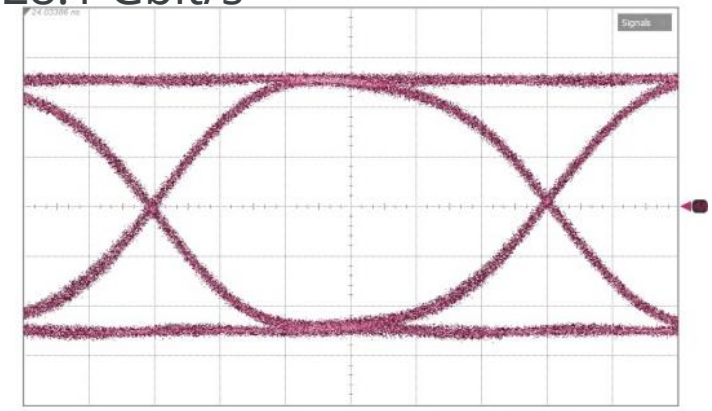
32.1 Gbit/s



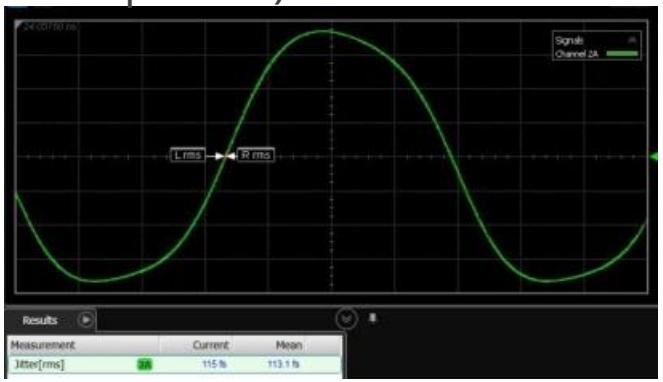
21 Gbit/s



28.1 Gbit/s



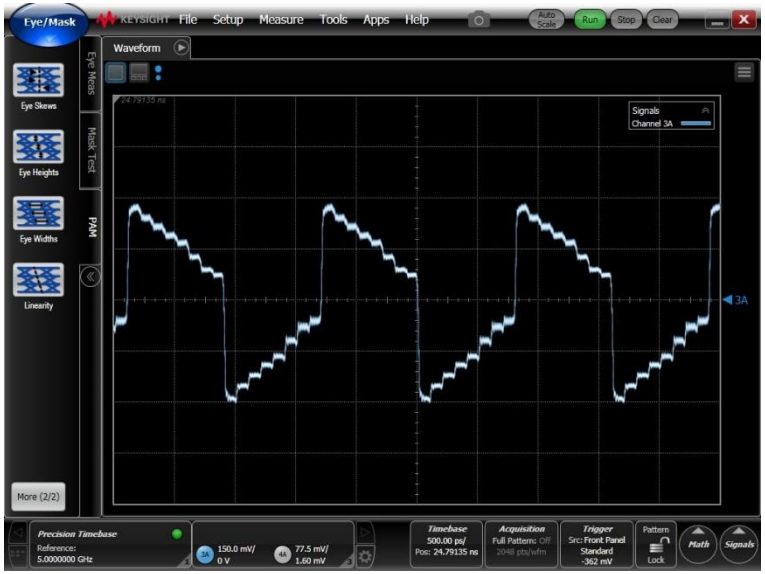
Low Intrinsic Jitter 115 fs (rms) @ 28.1 Gbit/s ("1010..." pattern)



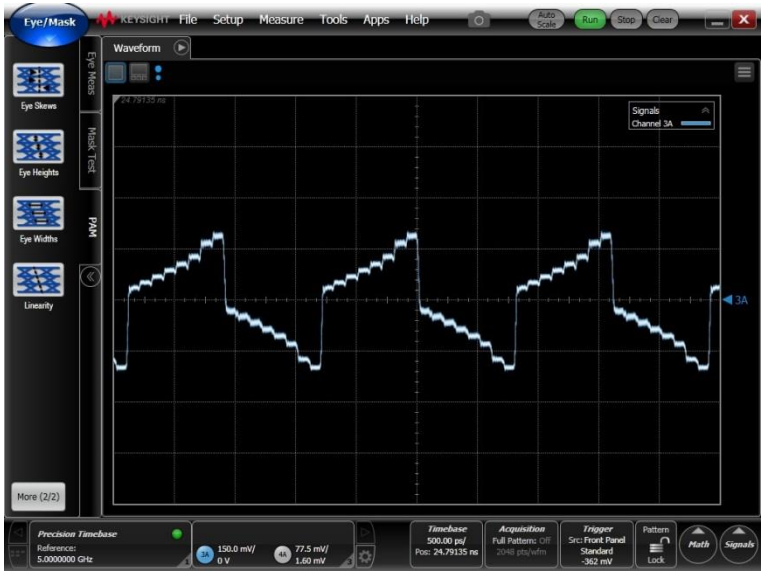
MU195020A PPG Data Output 10Tap Emphasis

Flexible Support for High-speed Device with Long-channel Design Evaluations

- 10Tap Emphasis
- Control up to 20 dB
- Pre-Emphasis output with peak output amplitude of 1.5 Vp-p



Waveform for correcting transmission path loss



Waveform emulating signal loss

Voltage control at each 1 bit for 10-bit time period

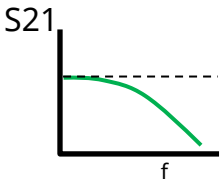
MU195020A Data Output　Variable ISI

Shorter Development Period by Eliminating Need for Multiple Test PC Boards

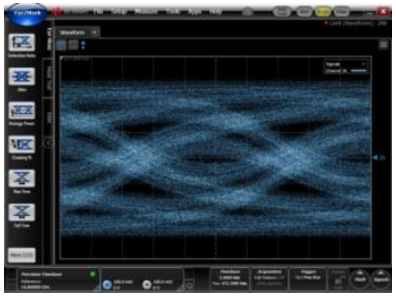
Simple and High-Reproducibility Design Tests of High-Speed Device Channel Loss Dependency

- Emulate channel loss by controlling Emphasis and generate loss-compensated signals
- Automatically calculate Emphasis setting using S-parameter

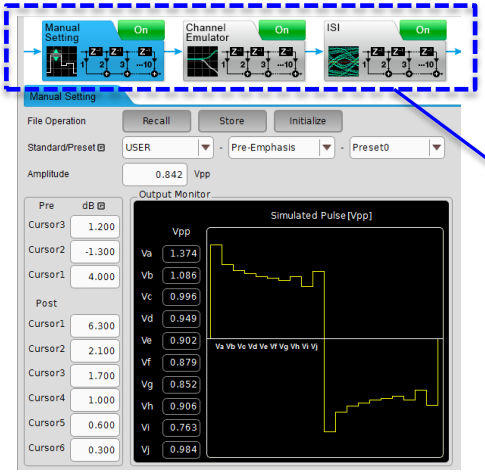
MP1900A SQA-R



Emulate channel loss
And generate loss-compensated signals (Variable ISI option)



CEI-28G, 14 dB loss typical waveform (ISI function)



・**Manual Setting:**
Correct signal for target Eye Height/Width using 10Tap Emphasis function
・**Channel Emulator:**
Emulate S2P and S4P data loss insertion, and perform Emphasis compensation
・**ISI:**
Emulate ISI using CEI-28G/25G Nyquist frequency loss setting

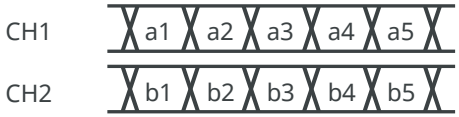
MU195020A PPG Multi-channel

Multiplexing, high-bit-rate and crosstalk tests are supported by the multi-channel Data output, pattern synchronization and skew control functions for easy flexible evaluations of future high-bit-rate and multi-channel interfaces.

Sync Channel Number	Supported Function	Application	Equipment Configuration
2ch	2ch Combination	32G PAM4 Generation 2:1 MUX Evaluation	MU195020A 2ch PPG x1
	Channel Synchronization		
4ch	64G x 2ch Combination	64G PAM4 Generation 4:1 MUX Evaluation	MU195020A 2ch PPG x2
	Channel Synchronization	QSFP28 Evaluation	

・2ch Combination

Supports shift to “a1b1 a2b2 . . .” pattern and PAM4 output.



・64G x 2ch Combination

Supports shift to “a1b1c1d1 a2b2c2d2 . . .” pattern and 64 Gbaud PAM4 output from two 32G PPG units, 4CH.

・Channel Synchronization

One 16ch MP1900A supports parallel interface evaluations, crosstalk tests and D/A converter evaluations as well as synchronized output for up to four MP1900A units.

21G/32G bit/s SI ED MU195040A Features

- Bit rate of 2.4 to 21 Gbit/s or 32.1 Gbit/s
- 1ch/2ch selection
- Built-in multi-band CTLE function
  - Peak frequency: 14, 8, 4 GHz switchable
  - Gain control: 0 to –12 dB control
- Data input amplitude: 0.05 to 1.0 Vp-p (Single-end)
- Input sensitivity @ 28.1Gbit/s NRZ: 15 mV (Eye Height) (typ.); 22 mVp-p (Eye amplitude)
  @ 28.1Gbit/s PAM4: 30 mV/Eye(Eye Height) (typ.); 150 mVp-p (Eye amplitude)
- Auto-measurements (Auto-search/Adjust, Eye Contour, Bathtub, Jitter Tolerance)
- Clock Recovery: 2.4 to 32.1 Gbit/s, SSC support
- PCI Express Link Training

MU195040A　21G/32G bit/s SI ED

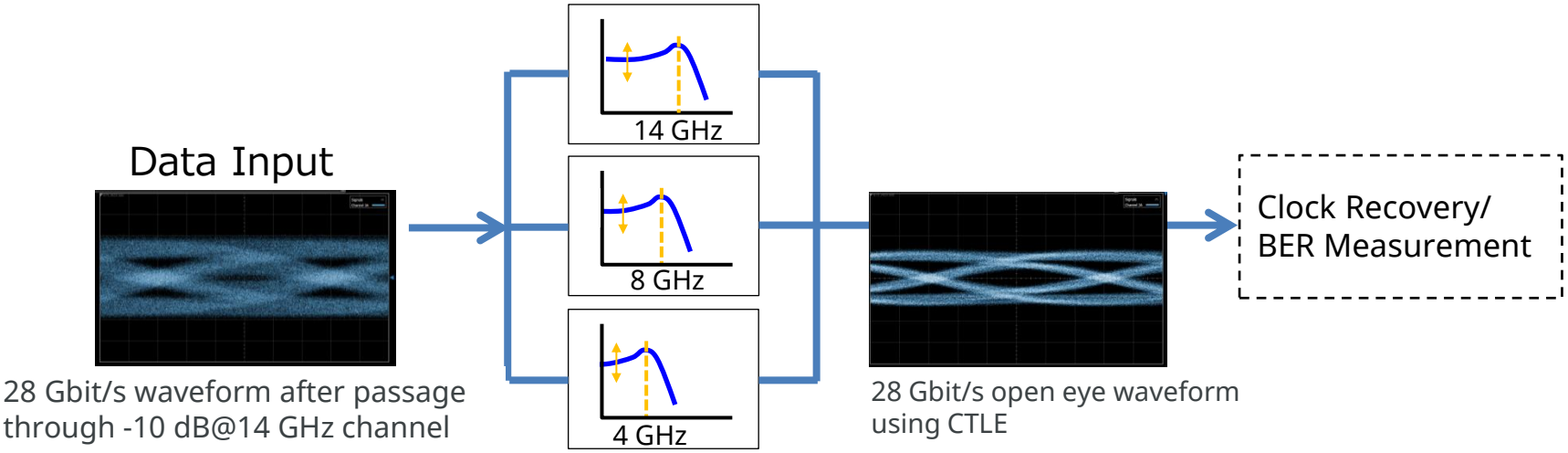
Data1 (differential)　**Data2 (differential)**

- **Multi-band CTLE**
- **High-sensitivity input**
- **CDR supporting SSC**

DUT

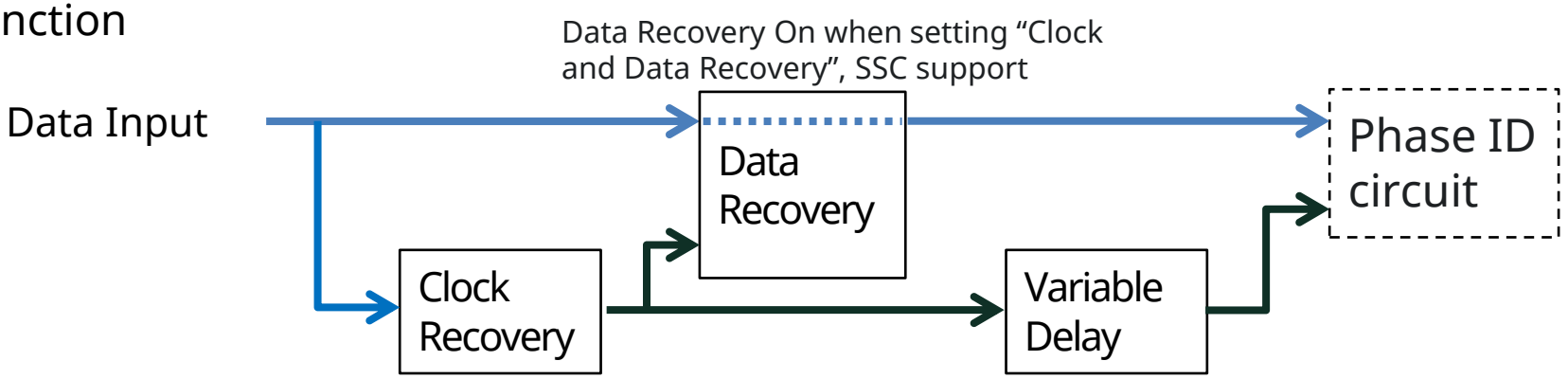
MU195040A ED Data Input CTLE/Clock Recovery Functions

Supports input receiver measurements for CEI-28G, PCIe Gen 3 (8 GT/s), Gen4 (16 GT/s) using 3-band CTLE (peak frequency of 14, 8 , and 4 GHz)



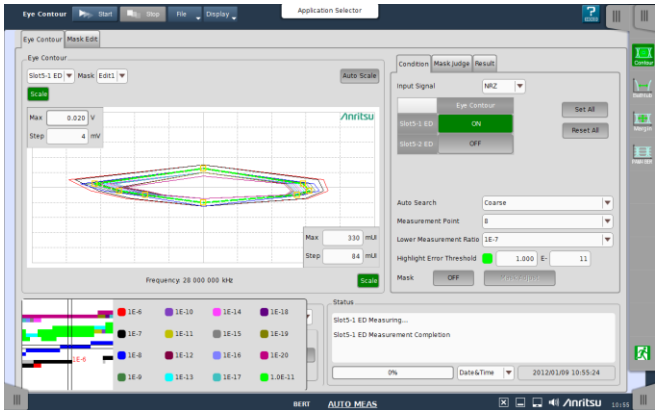
Supports SSC to implement Eye analysis for input signals with added Jitter

- 2.4 Gbit/s to 32.1 Gbit/s (extracts Clock from Data1 input signal)
- External Clock/Clock Recovery/Clock and Data Recovery_SSC support switching function

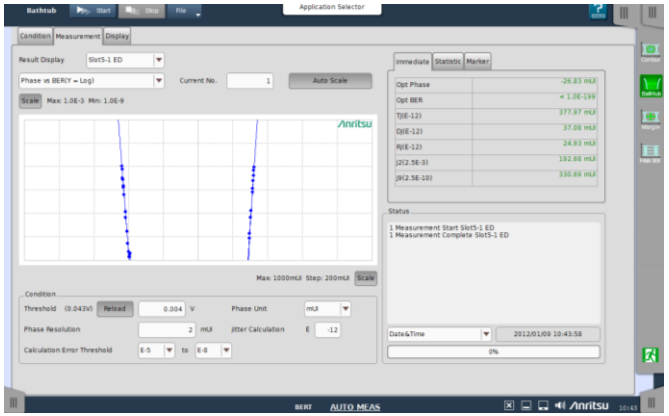


MU195040A ED Auto Measurement・Analysis Functions

Higher-accuracy Eye analysis is supported using the auto-measurement and auto-analysis functions, such as Auto Search/Auto Adjust, Bathtub, Eye Contour, Eye Margin, and PAM BER measurement that make use of the measurement high-input-sensitivity performance.



Example of Eye Contour Measurement at Input of Small 50 mVp-p Signal



Bathtub Measurement Example

Example of Eye Contour Measurement at Input of PAM4 Signal

Noise Generator MU195050A Features

Supports Voltage Noise Tolerance tests specified by CEI and IEEE802.3 for backplane, PCIe, and Thunderbolt measurements

- Noise addition to Data signals up to bit rates of 32.1 Gbit/s
- 2ch output
- CMI/DMI/White noise support
  - Common mode noise frequency: 0.1 GHz to 6 GHz
  - Differential mode noise frequency: 2 GHz to 10 GHz
  - White noise band: 10 GHz; Crest Factor: >5
- Supports external noise input

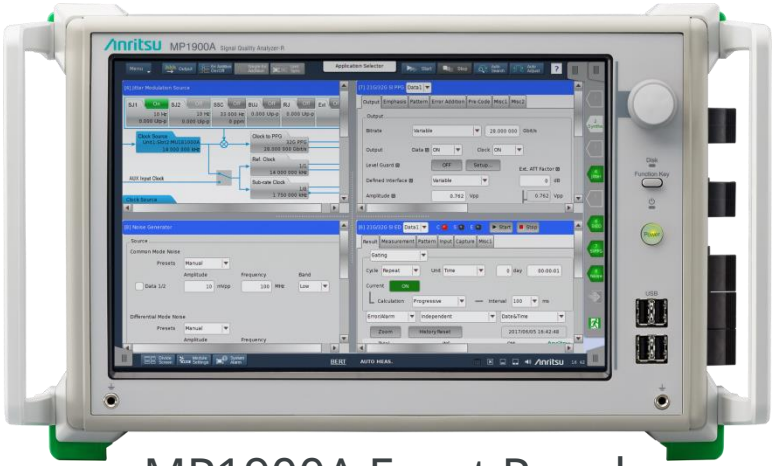
MU195020A

MU195050A
Noise Generator

・**Built-in CMI/DMI/White noise**
・**2ch output**

DUT

MP1900A Main Unit Features



MP1900A Front Panel

- 8 Slots
- Install up to eight 2ch PPG and ED modules
- Synchronize up to four MP1900A main units → Expansion to 2 Tbit/s
- Backwards compatibility with existing MP1800A modules

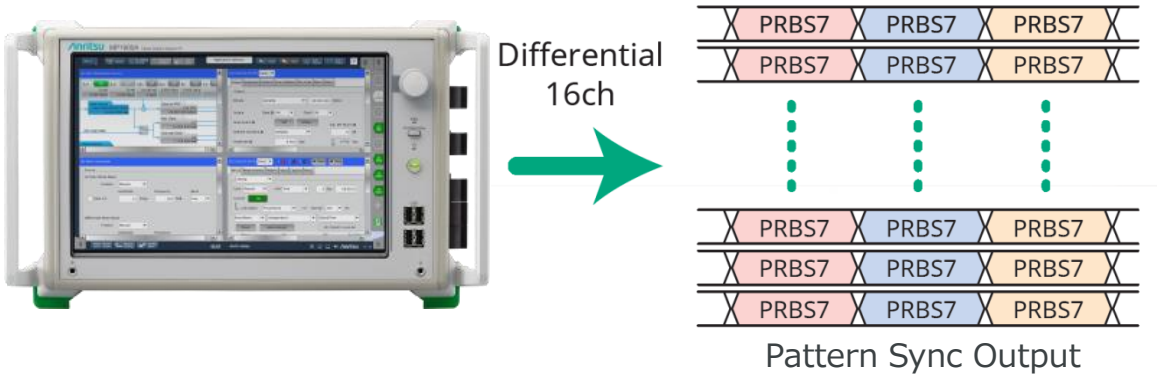
MP1900A Side Panel

- Touch Screen
- GPIB x 1, and Ethernet x 2
- USB x 6, HDMI x 1, and D-SUB x 1
- Windows Embedded Standard 7

MP1900A 8-slot Main Unit Expandability

Future-proof Main Unit Expandability

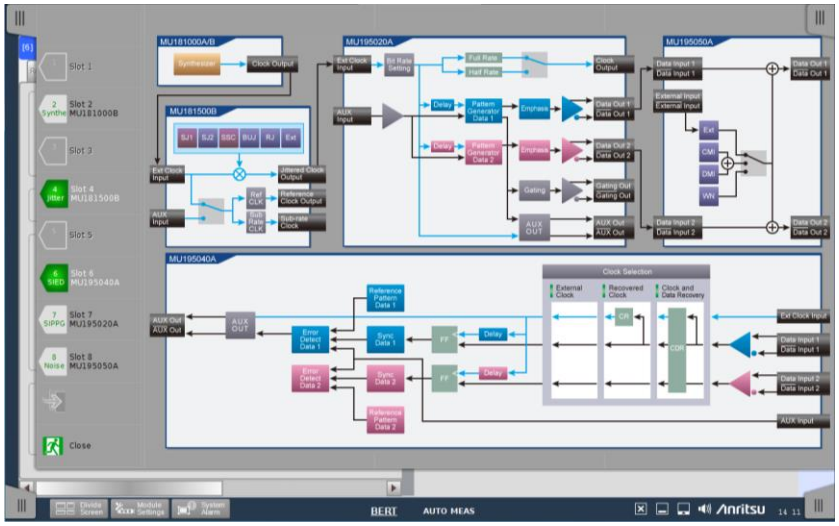
- One Main Unit Supports 16ch Transmissions for Future High Bit Rates



- Multi-channel Synchronized Output of Four MP1900A Main Units

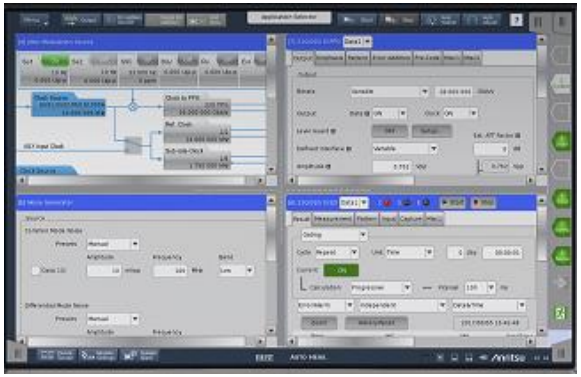
System View User Interface and Improved Operability using Multiple Windows

Operability is improved by the large 12.1-inch LCD touch panel and intuitive GUI. The newly developed System View user interface displays easy-to-understand system function blocks with help guidance for system settings and easy operation of each module.



System View User Interface

Setup Instructions



4ch Multi-channel Measurement Results on One Screen

MP1900A PAM4 Applications

Standards for High-Speed Interconnects using PAM4

Optical Interface

Standard		Distance	Format	Baud Rate
400G	400G BASE-SR16	100 m	NRZ	26.6G
	400G BASE-DR4	**500 m**	**PAM4**	**53.1G**
	400G BASE-FR8	**2 km**	**PAM4**	**26.6G**
	400G BASE-LR8	**10 km**	**PAM4**	**26.6G**
200G	**200G BASE-SR4**	**100 m**	**PAM4**	**26.6G**
	200G BASE-DR4	**500 m**	**PAM4**	**26.6G**
	200G BASE-FR4	**2 km**	**PAM4**	**26.6G**
	200G BASE-LR4	**10 km**	**PAM4**	**26.6G**
100G	100G BASE-SR10	100/150 m	NRZ	10.3G
	100G BASE-SR2	**100 m**	**PAM4**	**26.6G**
	100G BASE-DR	**500 m**	**PAM4**	**53.1G**
	100G BASE-SR4	70/100 m	NRZ	25.8G
	100G SWDM	400 m	NRZ	25.8G
	100G PSM4	500 m	NRZ	25.8G
	CWDM4/CLR4	2 km	NRZ	25.8G
	100G BASE-LR4	10 km	NRZ	25.8G
	100G BASE-ER4	40 km	NRZ	25.8G
50G	**50G BASE-SR**	**100 m**	**PAM4**	**26.6G**
	50G BASE-FR	**2 km**	**PAM4**	**26.6G**
	50G BASE-LR	**10 km**	**PAM4**	**26.6G**
25G	25G BASE-SR	100 m	NRZ	25.8G
	25G BASE-FR	2 km	NRZ	25.8G
	25G BASE-LR	10 km	NRZ	25.8G

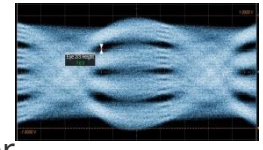
Electrical Interface

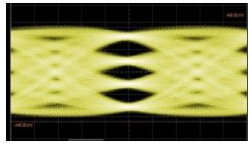
Standard IEEE802.3bs, OIF-CEI		Format	Baud Rate
400G	400GAUI-16	NRZ	26.6G
	400GAUI-8	**PAM4**	**26.6G**
200G	200GAUI-8	NRZ	26.6G
	200GAUI-4	**PAM4**	**26.6G**
100G	CAUI-10	NRZ	10.3G
	CAUI-4	NRZ	25.8G
50G	**50GAUI**	**PAM4**	**26.6G**
25G	25GAUI	NRZ	25.8G

Standard IEEE802.3by, IEEE802.3cd		Format	Baud Rate
200G	**200G BASE-CR4**	**PAM4**	**26.6G**
	200G BASE-KR4	**PAM4**	**26.6G**
100G	100G BASE-CR4	NRZ	25.8G
	100G BASE-KR4	NRZ	25.8G
	100G BASE-KP4	**PAM4**	**13.6G**
	100G BASE-CR2	**PAM4**	**26.6G**
	100G BASE-KR2	**PAM4**	**26.6G**
50G	**50G BASE-CR**	**PAM4**	**26.6G**
	50G BASE-KR	**PAM4**	**26.6G**

Outline of MP1900A 32 Gbaud PAM4 BER Solution

MP1900A





32 Gbaud Power PAM4 Converter
G0375A

Loss CH

DUT

32 Gbaud PAM4 Decoder with CTLE
G0376A

Supports PAM4 BER Measurements of PRBS31Q Pattern

- Small remote head for close-in approach to DUT
- Multi-channel
- Excellent expandability and PAM4/NRZ support

- 3.9 Vp-p (differential) PAM4 output
- 10Tap Emphasis
- Clean Eye/Low Jitter
- Tr/Tf 14 ps (typ.) (PAM4 output)

- CTLE 14 GHz, 12 dB
- Clock Recovery (by MU195040B ED)
- High input sensitivity of 40 mV(EH)
- True PAM4 BER measurement

PAM4 BER Measurement using MP1900A Series + G0375A/G0376A

Combining the 32G 2ch BERT (MSB/LSB, 2ch Combination) and PAM4 Converter/Decoder supports both PAM4 and NRZ BER measurements.

PPG1 0 0 2 2 2 0 2 0 . . . (MSB)

PPG2 0 1 0 1 0 0 1 1 . . . (LSB)

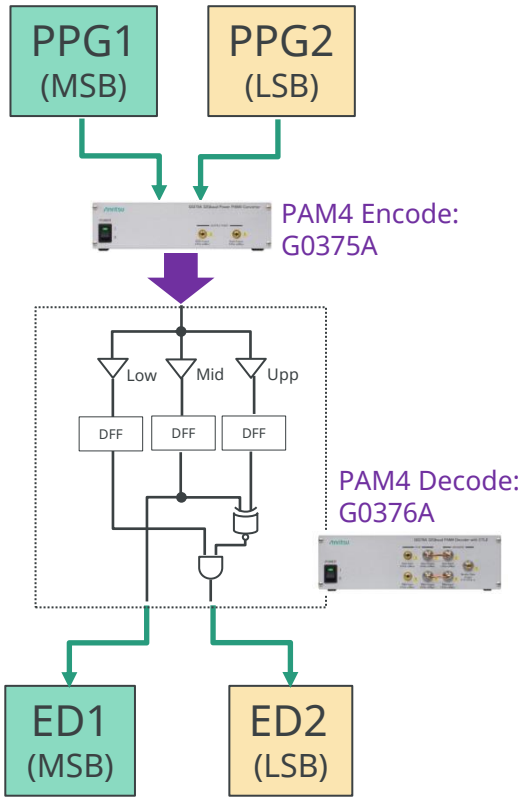
(PAM4 Encode: **G0375A**)

PAM4 **0 1 2 3 2 0 3 1 . . .**

(PAM4 Decode: **G0376A**)

ED1 0 0 1 1 1 0 1 0 . . . (MSB)

ED2 0 1 0 1 0 0 1 1 . . . (LSB)



PAM4 Test Patterns (1/2)

Support PAM4 Test Patterns Specified by 200/400 GbE Standards

- Supported Test Patterns

Supported Test Patterns	
PRBS13Q, PRBS31Q	QPRBS13-CEI
SSPRQ	PRBS
SSPR	JP03A, JP03B
Square	PRQS10
Transmitter Linearity Test Pattern	PrePRBS20, PreQPRBS13-CEI

- **Details**

PRBS13Q, PRBS31Q*, SSPRQ:

Patterns defined by IEEE802.3bs, 802.3cd 200 GbE, and 400 GbE

QPRBS13-CEI:

Transmitter Output measurement and Receiver Input calibration patterns defined by CEI-56G PAM4 standard

PRBS 7,9,10,11,15,20,23*,31*

Pseudo Random Bit Sequence pattern

SSPR (Short Stress Pattern Random)**:**

This 32,762-bit pattern is defined by CEI 3.1. The pattern length is equivalent to PRBS15 and it is used as a PAM4 evaluation pattern due to its features as a high-stress test signal.

PrePRBS20, PreQPRBS13:

The 1/(1+D) mod4 Precoding (defined in IEEE 802.3cd standard) pattern has been added to the PRBS20 and QPRBS13 patterns to reduce DFE burst errors at use by Tx.

*Supported by G0376A

PAM4 Test Patterns (2/2)

JP03A:

This “0303…” pattern string is used for evaluating Transmitter RJ.

JP03B:

This 62-symbol pattern has 15 repetitions of “03” followed by 16 repetitions “30”.

030303030303030303030303030303033030303030303030303030303030303030

It is used for evaluating Transmitter Even-Odd Jitter.

Square:

This “3333333300000000” pattern string is for Optical Modulation Amplitude (OMA) evaluation of optical interfaces.

Transmitter Linearity Test Pattern:

This 160-symbol pattern is composed of blocks of 10 PAM4 symbols shown below forming a contiguous pattern each of 16UI.

{0, 1, 2, 3, 0, 3, 0, 3, 2, 1}

The Linearity Test in the latest standards uses a PRBS13Q pattern.

R_{LM} = min((3 x ES1), (3 x ES2), (2 – 3 x ES1), (2 – 3 x ES2))

ES1 = $(V_1 - V_{mid})/(V_0 - V_{mid})$, ES2 = $(V_2 - V_{mid})/(V_3 - V_{mid})$, $V_{mid} = (V_0 + V_3)/2$

PRQS10:

This 4^{10}-1-bit length pattern for PAM4 test was discussed by IEEE 802.3bs.

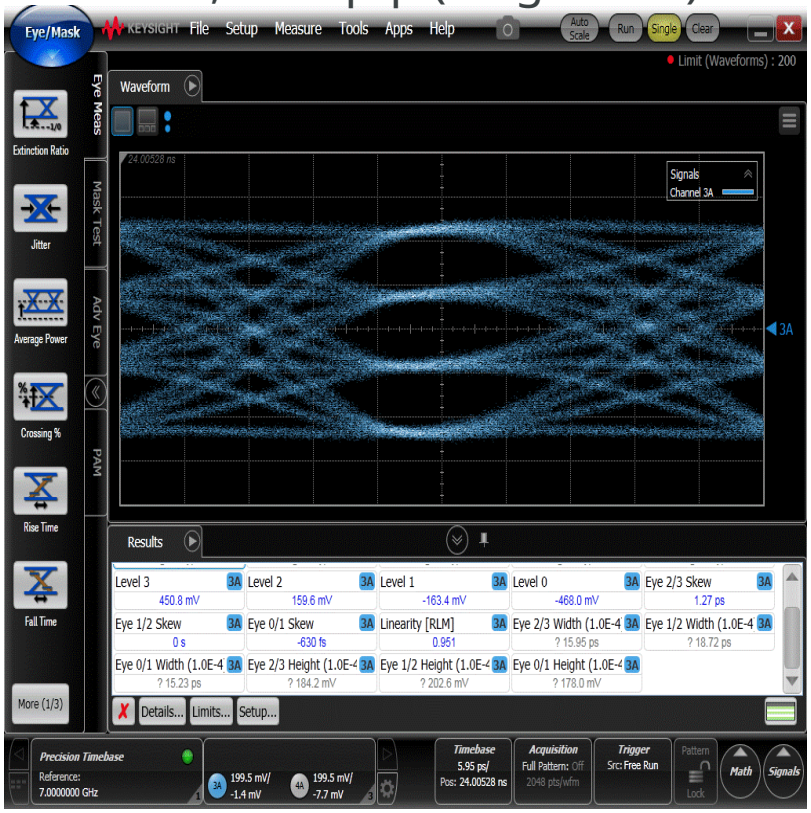
Gray-xxxx

Although PAM4 signals have four levels implemented as 2-bit pairs, sometimes a 2-bit change such as 01 to 10 is wrongly detected for a 1 level change. To prevent this, the Tx side uses a Gray code (00→00, 01→01, 10→11, 11→10) and the Rx side uses the opposite Gray decode.

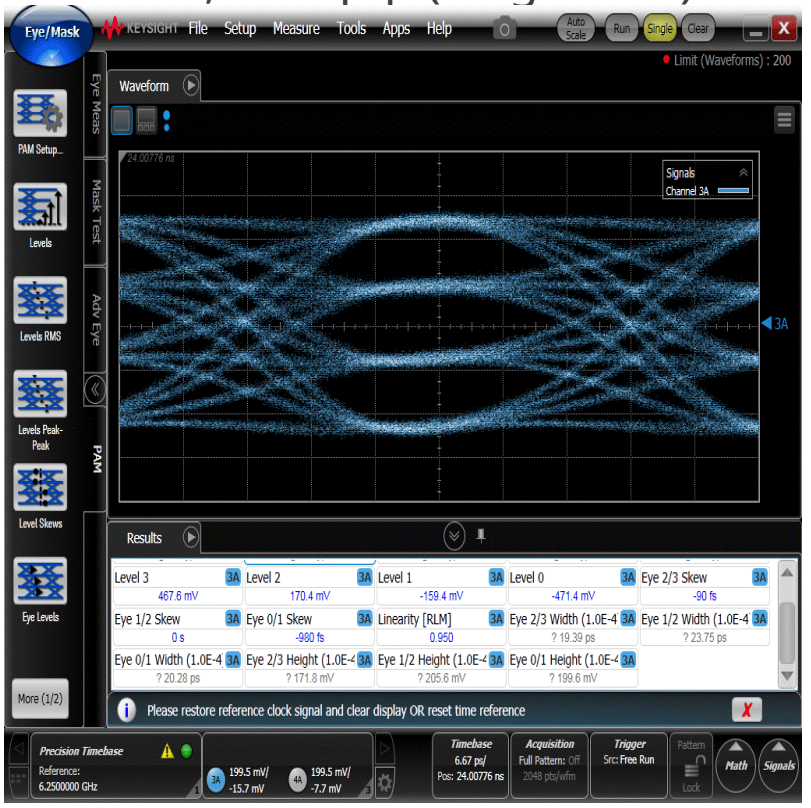
G0375A with MU195020A PPG PAM4 Typical Waveforms

Supports High-Reproducibility Evaluations using Low Intrinsic Jitter PAM4 Data Output

28 Gbaud, 0.9 Vp-p (Single-end)



25 Gbaud, 0.9 Vp-p (Single-end)



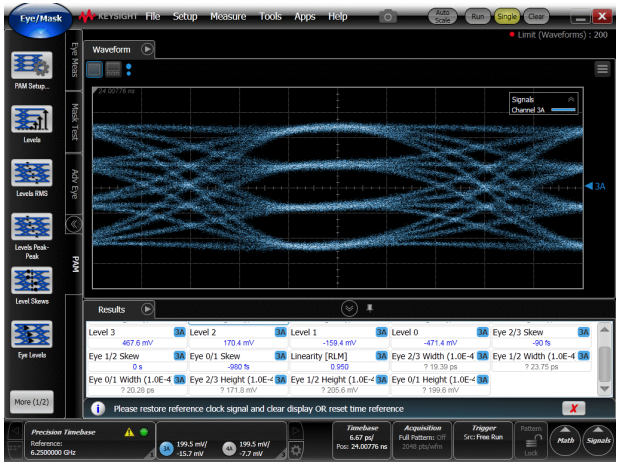
MU195020A Emphasis Pre1 = 0.5 dB, Post1 = 0.3 dB, 40 cm test cable

CEI-56G-VSR-PAM4 Receiver Evaluation Typical Test Signals

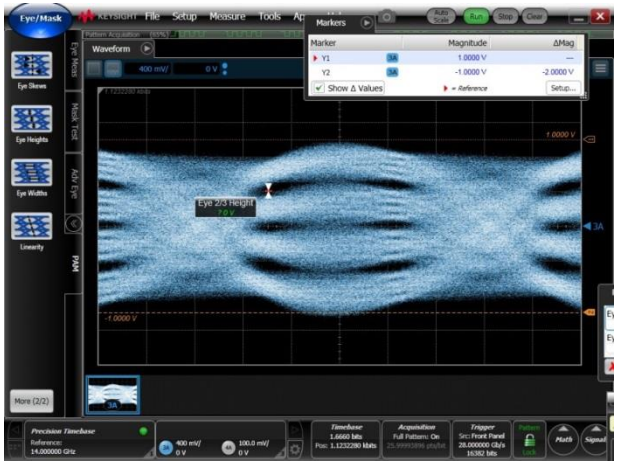
Supports PAM4 high-speed device receiver tests

- Low Jitter/Clean Eye
- PAM4 10Tap Emphasis function

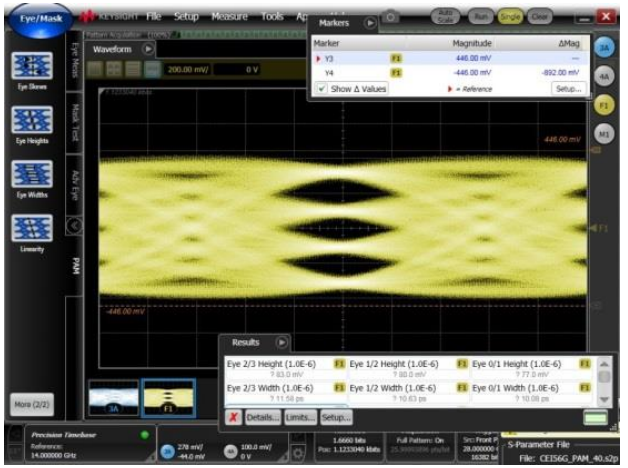
28 Gbaud Without Emphasis
(before passing channel)



28 Gbaud With Emphasis
(before passing –10 dB channel)



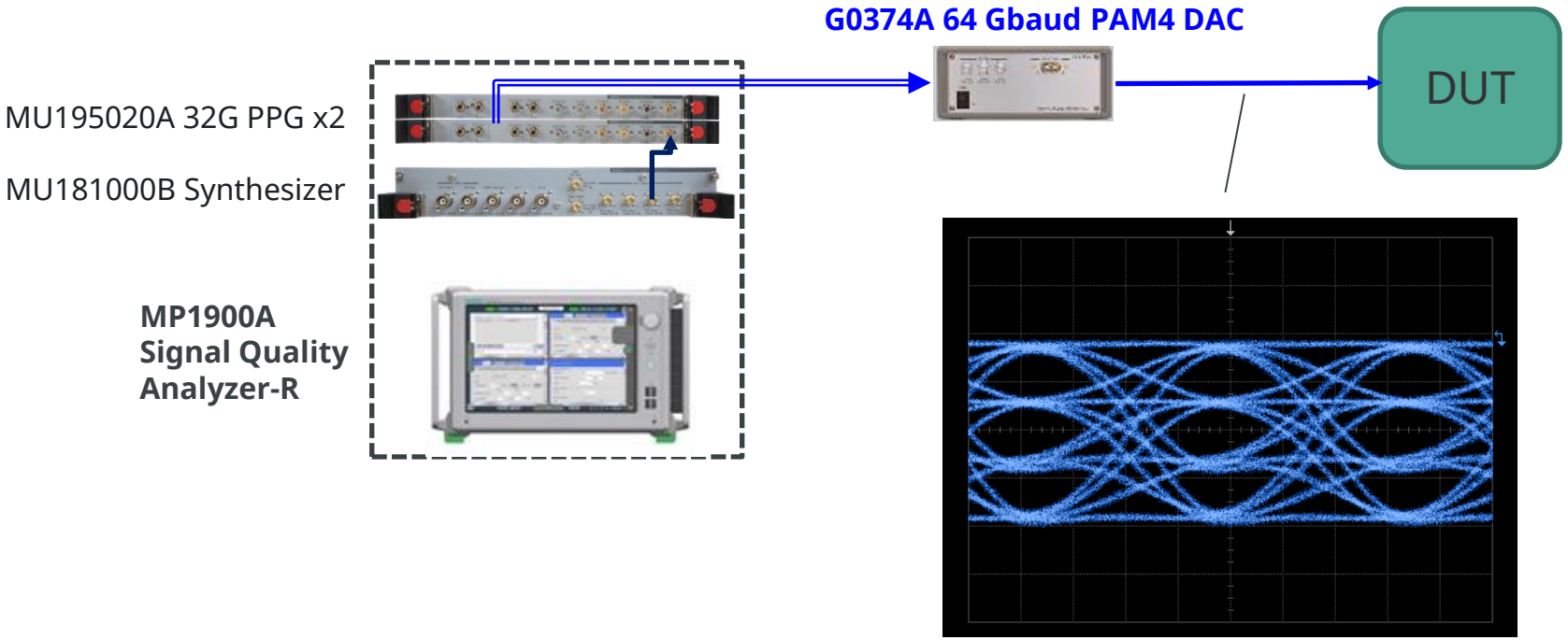
28 Gbaud With Emphasis
(after passing –10 dB channel)



MP1900A 64 Gbaud PAM4 Signal Generation

Easy and effective expandability for high baud-rate PAM4

- Expandability
- 64 Gbaud(maximum) high baud-rate
- 1.4 Vp-p (diff. typ.) output
- Remote-head
- Clean Jitter signal



64Gbaud PAM4 Typical Waveform

32 G PAM4 BER Measurement Recommended Equipment List

Model	Name	Option	Qty	Remark
G0375A	32Gbaud Power PAM4 Converter	-	1	
G0376A	32Gbaud PAM4 Decoder with CTLE	-	1	
MP1900A	Signal Quality Analyzer-R	-	1	
MU181000B	12.5GHz 4port Synthesizer	-	1	
MU181500B	Jitter Modulation Source	-	1	For Jitter Tolerance Test
MU195020A	21G/32G bit/s SI PPG	001, 020, 021, 031	1	
MU195040A	21G/32G bit/s SI ED	001, 020, 022	1	
J1439A	Coaxial Cable (0.8m, K connector)		1	
J1728A	Electrical Length Specified Coaxial Cable (0.4m, K connector)	-	(2)	Cable for waveform monitoring
MX183000A PAM4 Control	PAM4 Control		1	Standard software
MX183000A-PL001	Jitter Tolerance Test		1	For Jitter Tolerance Test

64 G PAM4 Signal Generation Recommended Equipment List

Model	Name	Option	Qty	Remark
G0374A	64Gbaud PAM4 DAC	-	1	
MP1900A	Signal Quality Analyzer-R	-	1	
MU181000B	12.5GHz 4port Synthesizer	-	1	
MU181500B	Jitter Modulation Source	-	1	For Jitter Tolerance Test
MU195020A	21G/32G bit/s SI PPG	001, 020, 031	2	

MP1900A PCI Express and USB3.1 Applications

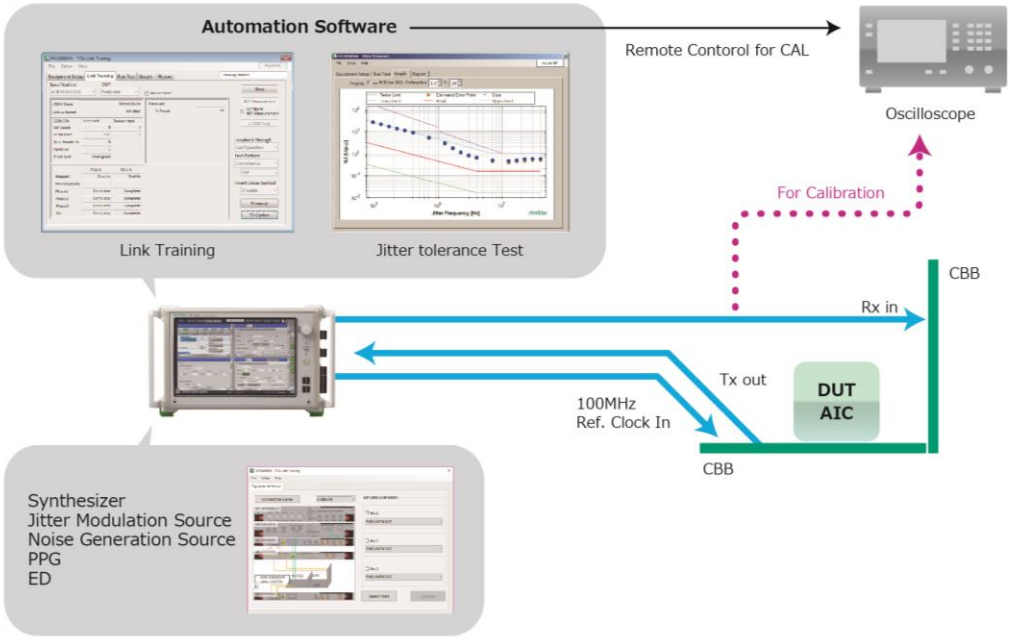
MP1900A Series PCI Express Test Solution

Measurement Item	Supported Software
Transmitter Test	*
Tx Response Time	MX183000A-PL021
Stressed Signal Calibration	*
Transition to Loopback State	MX183000A-PL011, PL021
Rx Link Equalization Test	MX183000A-PL021
Jitter Tolerance Test	MX183000A-PL001
PLL Loop Bandwidth Test	*

* Contact your sales representative about expected future support.

MP1900A Series PCI Express Receiver Test Solution

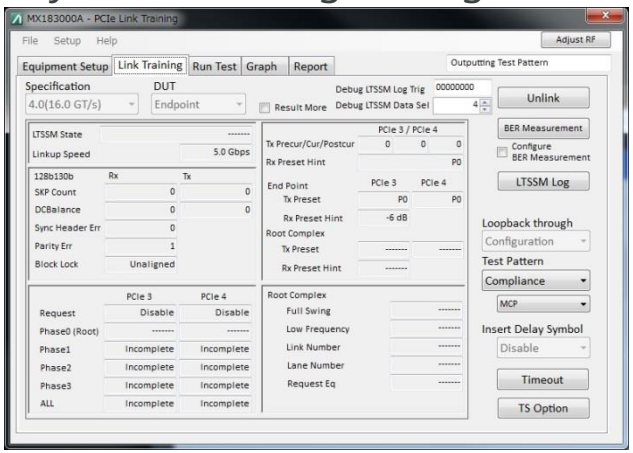
- All-in-one PCI Express Gen1 to 5 solution
- Wideband bit rate of 2.4 Gbit/s to 32.1 Gbit/s
  No need for hardware upgrade to support future Gen5 (32 GT/s)
- Automated LEQ test (Protocol Aware) with LTSSM event trigger function
- Low-Jitter test signals and high-input sensitivity performance
- Link Training and LTSSM analysis function
- SKP Order set and 8B/10B, 128B/130B coding
- Built-in noise (CMI and DMI) and Jitter (SJ, RJ, BUJ and SSC) addition function
- Supports both Common (MU181000B-002) and Separate Clock architectures



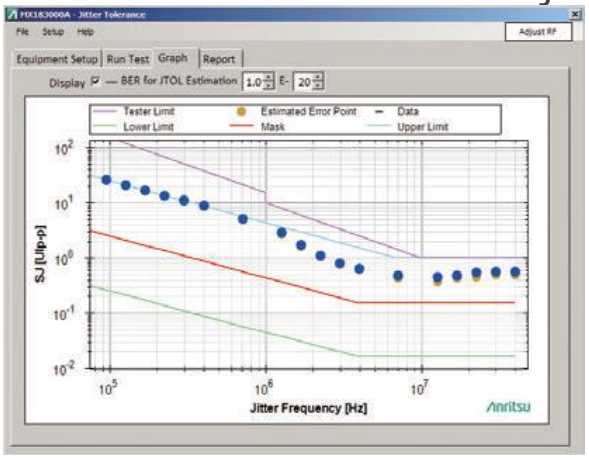
PCI Express Link Training, LTSSM Analysis and Jitter Tolerance Measurements (1/3)

Combining the PCIe Link Training MX183000A-PL021 and Jitter Tolerance Test MX183000A-PL001 software supports tests from the Link with the DUT to the Jitter Tolerance test measurements required by PCI Express receiver tests.

Displays Link Training Settings and Results



Automatic Measurement of Receiver Jitter Tolerance

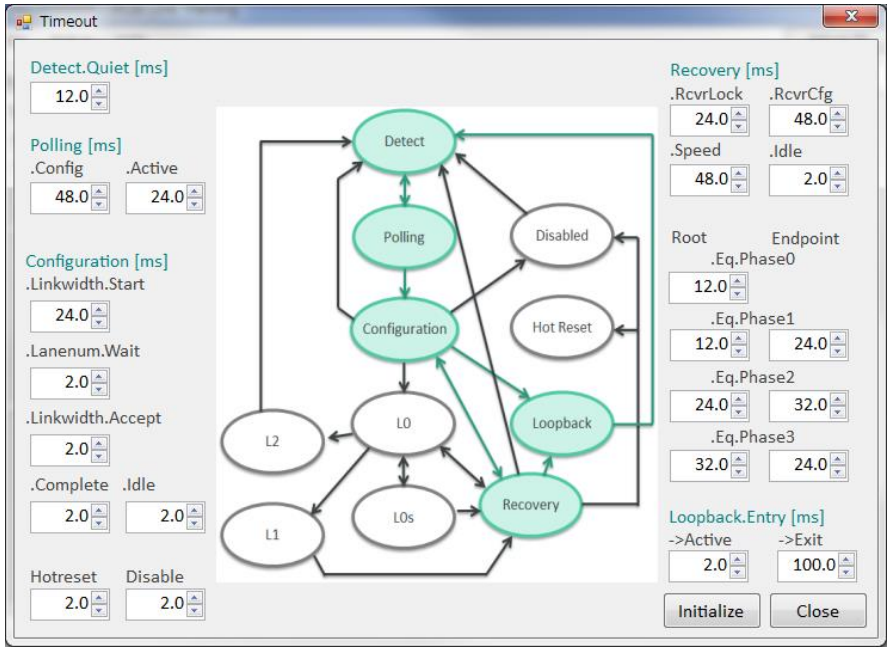


Item	MX183000A-PL021 Specifications
Supported Standard	PCI Express Rev 1.x (2.5 GT/s), 2.0 (5 GT/s), 3.x (8 GT/s), 4.0 (16 GT/s)
Test Pattern	Compliance (MCP, CP), PRBS (7, 9, 10, 11, 15, 20, 23, 31)
LTSSM State	Transition to Detect, Polling, Configuration, Recovery, Loopback
Loopback Through	Configuration, Recovery
TS Setting Parameters	SKP Insertion, 8B/10B, 128B/130B, FTS, Link Number, Lane Number, Scrambling

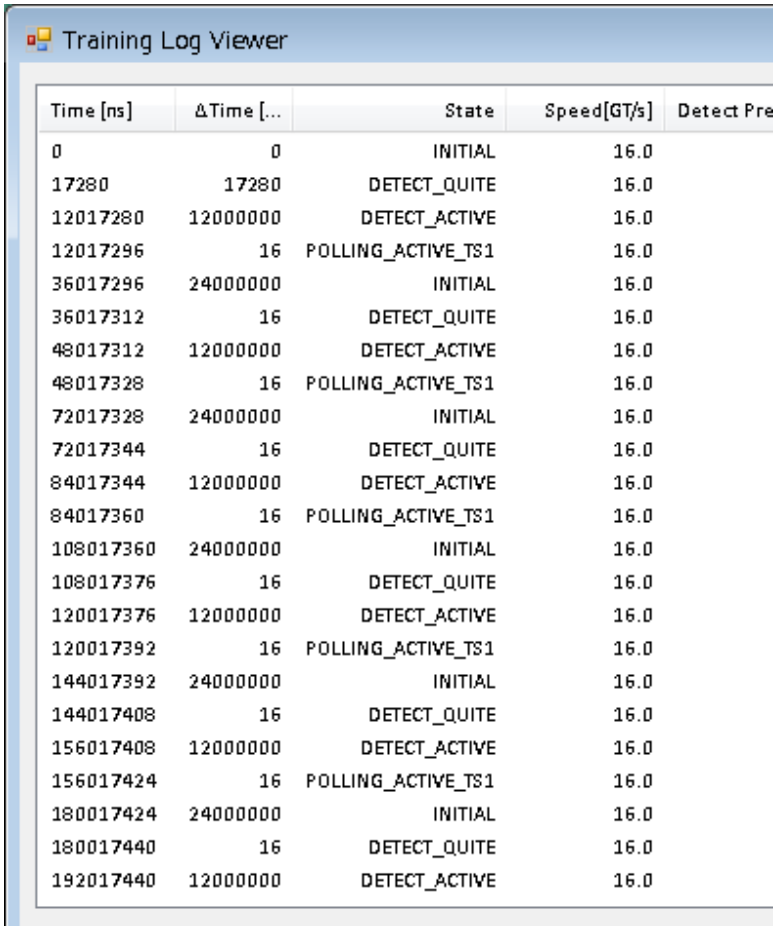
PCI Express Link Training, LTSSM Analysis and Jitter Tolerance Measurements (2/3)

Shorter Development Period by LTSSM Analysis Functions for Troubleshooting Cause of Link Faults

Examine each state transition time and path from “Detect” to ”Loopback”.



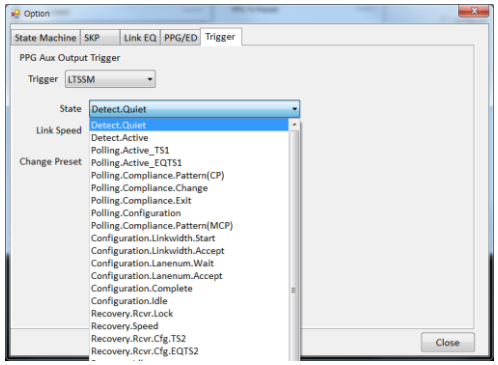
Check results for each state transition using Training Log Viewer.

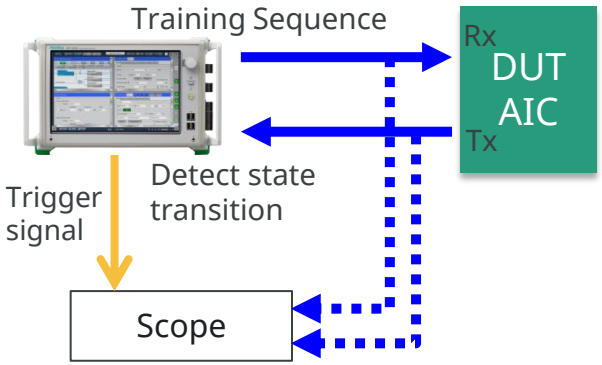


Time [ns]	ΔTime [...	State	Speed[GT/s]	Detect Pre
0	0	INITIAL	16.0	
17280	17280	DETECT_QUITE	16.0	
12017280	12000000	DETECT_ACTIVE	16.0	
12017296	16	POLLING_ACTIVE_TS1	16.0	
36017296	24000000	INITIAL	16.0	
36017312	16	DETECT_QUITE	16.0	
48017312	12000000	DETECT_ACTIVE	16.0	
48017328	16	POLLING_ACTIVE_TS1	16.0	
72017328	24000000	INITIAL	16.0	
72017344	16	DETECT_QUITE	16.0	
84017344	12000000	DETECT_ACTIVE	16.0	
84017360	16	POLLING_ACTIVE_TS1	16.0	
108017360	24000000	INITIAL	16.0	
108017376	16	DETECT_QUITE	16.0	
120017376	12000000	DETECT_ACTIVE	16.0	
120017392	16	POLLING_ACTIVE_TS1	16.0	
144017392	24000000	INITIAL	16.0	
144017408	16	DETECT_QUITE	16.0	
156017408	12000000	DETECT_ACTIVE	16.0	
156017424	16	POLLING_ACTIVE_TS1	16.0	
180017424	24000000	INITIAL	16.0	
180017440	16	DETECT_QUITE	16.0	
192017440	12000000	DETECT_ACTIVE	16.0	

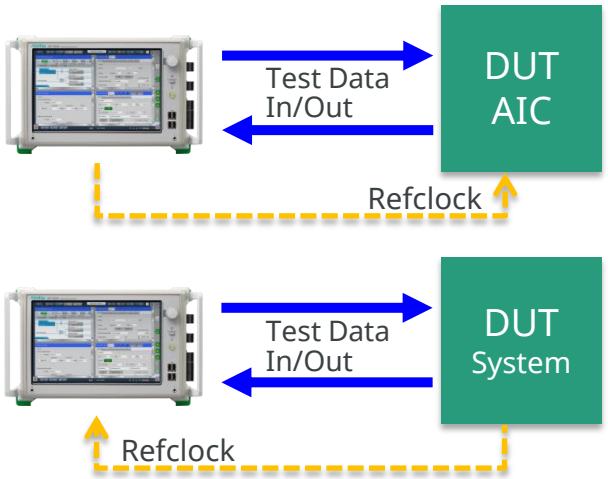
PCI Express Link Training, LTSSM Analysis and Jitter Tolerance Measurements (3/3)

Generate trigger at LTSSM transition timing to support examination using oscilloscope waveform.





Supports both common and separate Refclock test architectures and SRIS

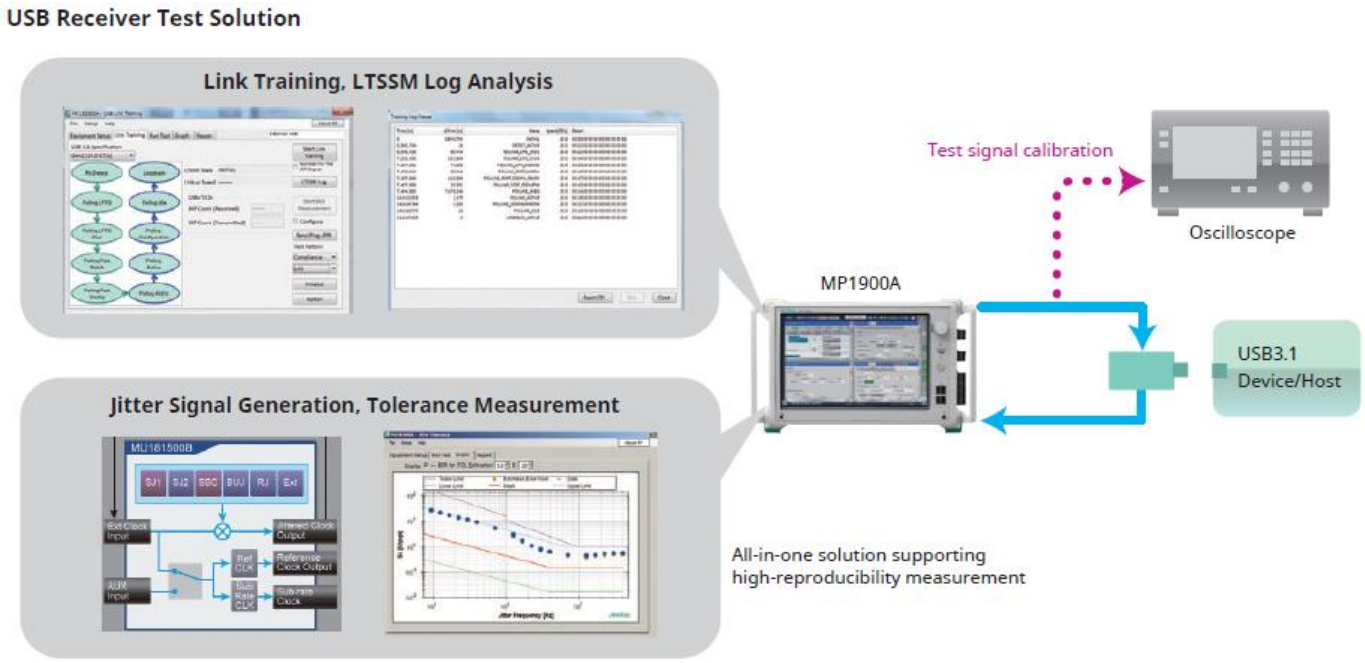


PCI Express Gen4 Receiver Test Recommended Equipment List

Model	Name	Option	Qty	Remark
MP1900A	Signal Quality Analyzer-R	-	1	
MU181000B	12.5GHz 4port Synthesizer	002	1	
MU181500B	Jitter Modulation Source	-	1	
MU195020A	21G/32G bit/s SI PPG	010, 011	1	Add Opt-001 for expansion to Gen5 (32 GT/s)
MU195040A	21G/32G bit/s SI ED	010, 011, 022	1	
MU195050A	Noise Generator	-	1	
MX183000A-PL001	Jitter Tolerance Test	-	1	
MX183000A-PL021	PCIe Link Training	-	1	

MP1900A Series USB3.1 Receiver Test Solution

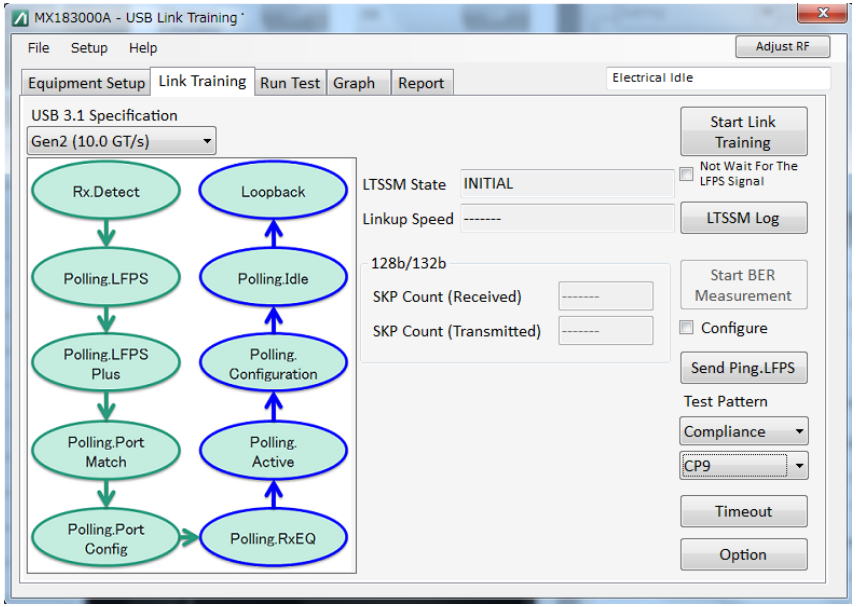
- Protocol Aware and All-in-one USB3.1 Rx test solution
- Wideband BERT 2.4 Gbit/s to 32.1 Gbit/s supporting PCIe Gen4 and Thunderbolt3
- High-quality waveforms with low Intrinsic Jitter, high-reproducibility measurement using high-sensitivity ED
- Link Training and LTSSM analysis function
- Transmit and receive LFPS and LBPM signals
- Insert and identify SKP Ordered Set
- Jitter Addition (SJ, RJ, BUJ, SSC) and Tolerance measurement



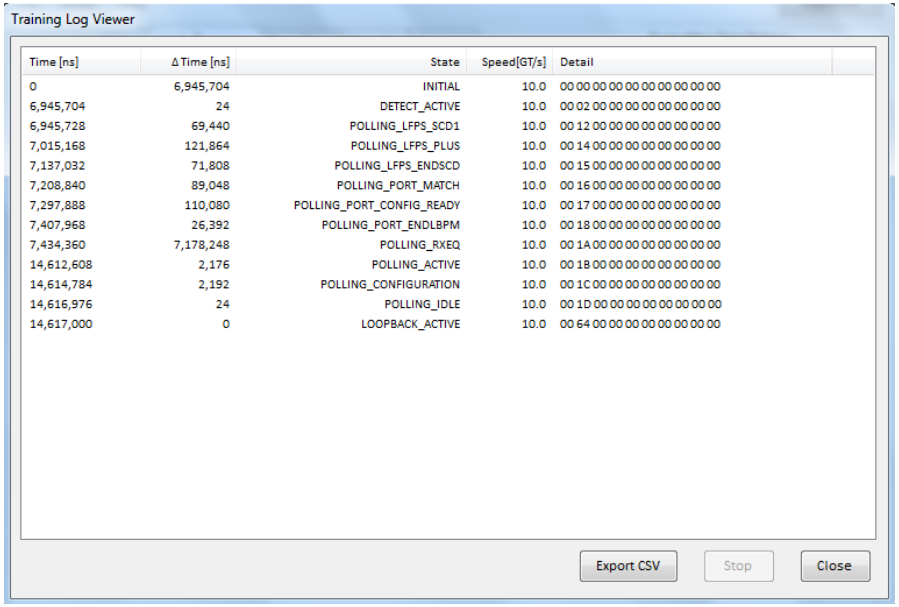
USB3.1 Link Training, LTSSM Analysis and Jitter Tolerance

Shorter Development Period by LTSSM Analysis Function for Troubleshooting Cause of Link Faults

Controls state transition from “Detect” to “Loopback” required by Rx test



For confirming results of each state transition with Training Log Viewer



USB3.1 Receiver Test Recommended Equipment List

Model	Name	Option	Qty	Remark
MP1900A	Signal Quality Analyzer-R	-	1	
MU181000B	12.5GHz 4port Synthesizer	-	1	
MU181500B	Jitter Modulation Source	-	1	
MU195020A	21G/32G bit/s SI PPG	010, 011	1	
MU195040A	21G/32G bit/s SI ED	010, 011, 022	1	
MU195050A	Noise Generator	-	1	Not required when using Pick Off Tee J1510A (2 pcs)
MX183000A-PL001	Jitter Tolerance Test	-	1	
MX183000A-PL022	USB Link Training	-	1	

Updated Functions

Software New Functions List

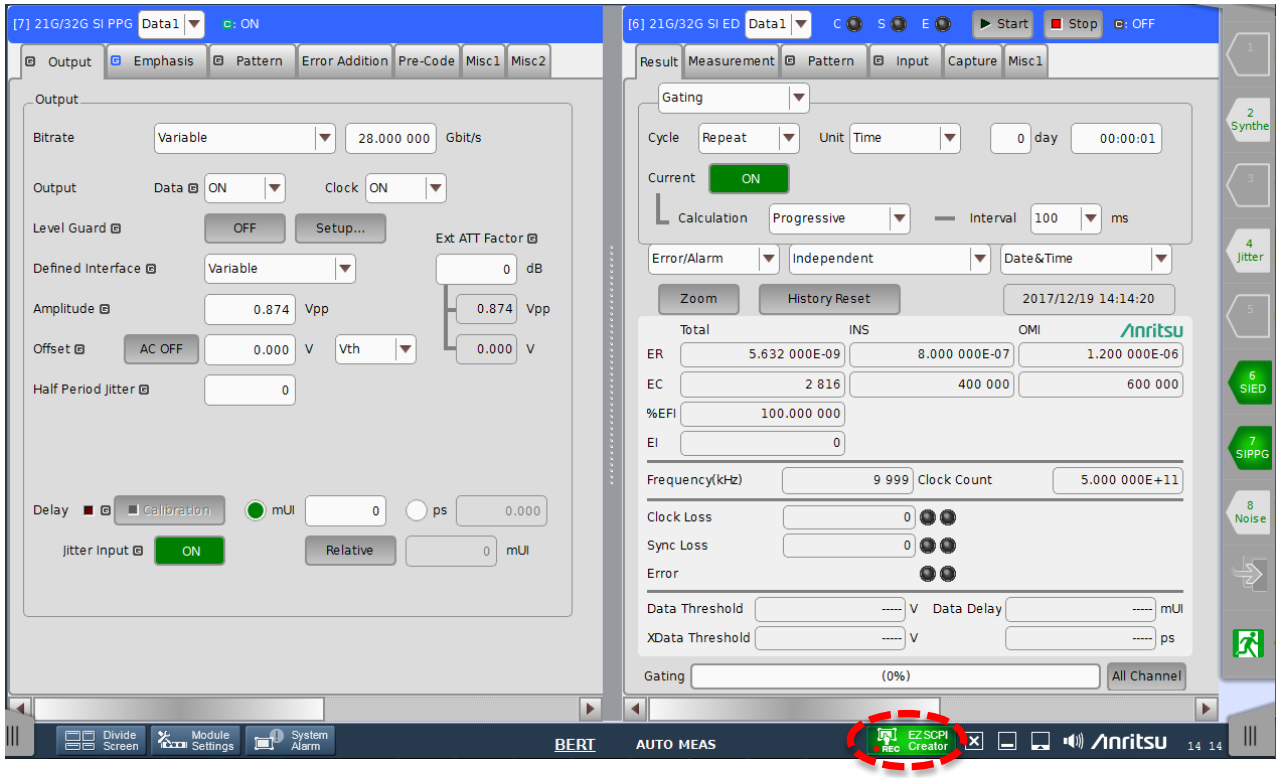
MX190000A Ver. 2 Added Functions	Remarks
EZ SCPI Creator	Remote command creation tool (Details in slide 45)
MU181500B Built-in SJ2 Addition	Adds MU181500B SJ2 function (Details in slide 46)
PAM4 Test Pattern Addition	Adds PRBS31Q and SSPRQ patterns
Install MU183020A and MU183040B in MP1900A	One each of MU183020A and MU183040B

MX183000A Ver. 3 Added Functions	Remarks
PL021 PCIe Link Training Link EQ Function Addition	Supports Link EQ function measurement (Details in slide 47)
PL021 PCIe Link Training LTSSM Trigger Function Addition	Generates trigger signal at LTSSM transitions (Details in slide 38)

EZ SCPI Creator

MX190000A
Ver. 2.00.00
Added Function

Operation while EZ SCPI Creator is ON creates remote command strings automatically, making it easy to describe remote commands.



EZ SCPI Creator ON

For example, executing the following operations:

- Set PPG Amplitude
- Set PPG Pattern Type
- Set PPG PRBS Length
- Set Output On
- Start ED measurement

Automatically generates these operation remote commands

```
:UENTry:ID 1; :MODule:ID 7; :INTerface:ID 1; :OUTPut:DATA:AMPLitude DATA,0.574
:UENTry:ID 1; :MODule:ID 7; :INTerface:ID 1; :SOURce:PATTern:TYPE PRBS
:UENTry:ID 1; :MODule:ID 7; :INTerface:ID 1; :SOURce:PATTern:PRBS:LENG 31
:SOURce:OUTPut:ASET ON
:UENTry:ID 1; :MODule:ID 6; :INTerface:ID 1; :SENSe:MEASure:STAR
```

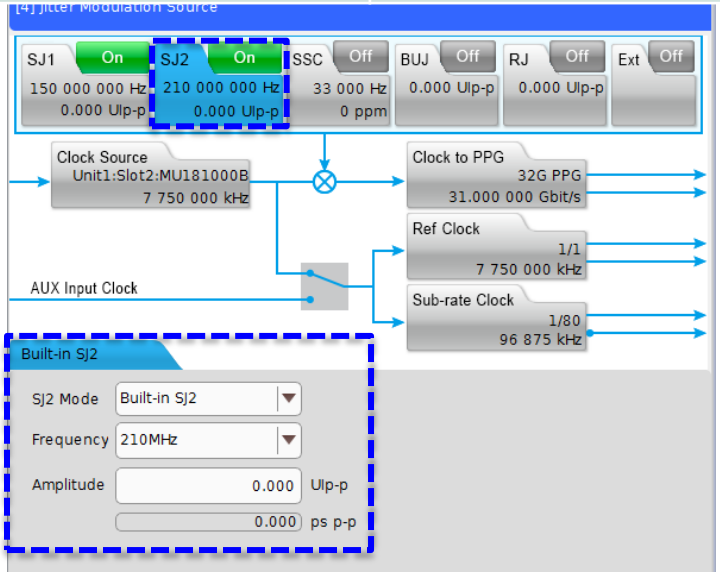
MU181500B Jitter Modulation Source Built-in SJ2 Support

MX190000A
Ver. 2.00.00
Added Function

One MU181500B unit can generate the following SJ2 (Built-in SJ2) in addition to SJ1.

SJ2 at other frequency ranges (10 Hz to 250 MHz) can be impressed by combined use with the MU181000B-001.

MU181500B Built-in SJ2 Frequency	Amplitude	Standard
33 kHz	0 to 500 UI at 8 Gbit/s 0 to 1000 UI at 16 Gbit/s	PCIe Gen3, 4 Base spec.
100 MHz	0 to 0.25 UI at 10 Gbit/s	USB3.1
210 MHz	0 to 0.2 UI at 16 Gbit/s	PCIe Gen4 Base spec.

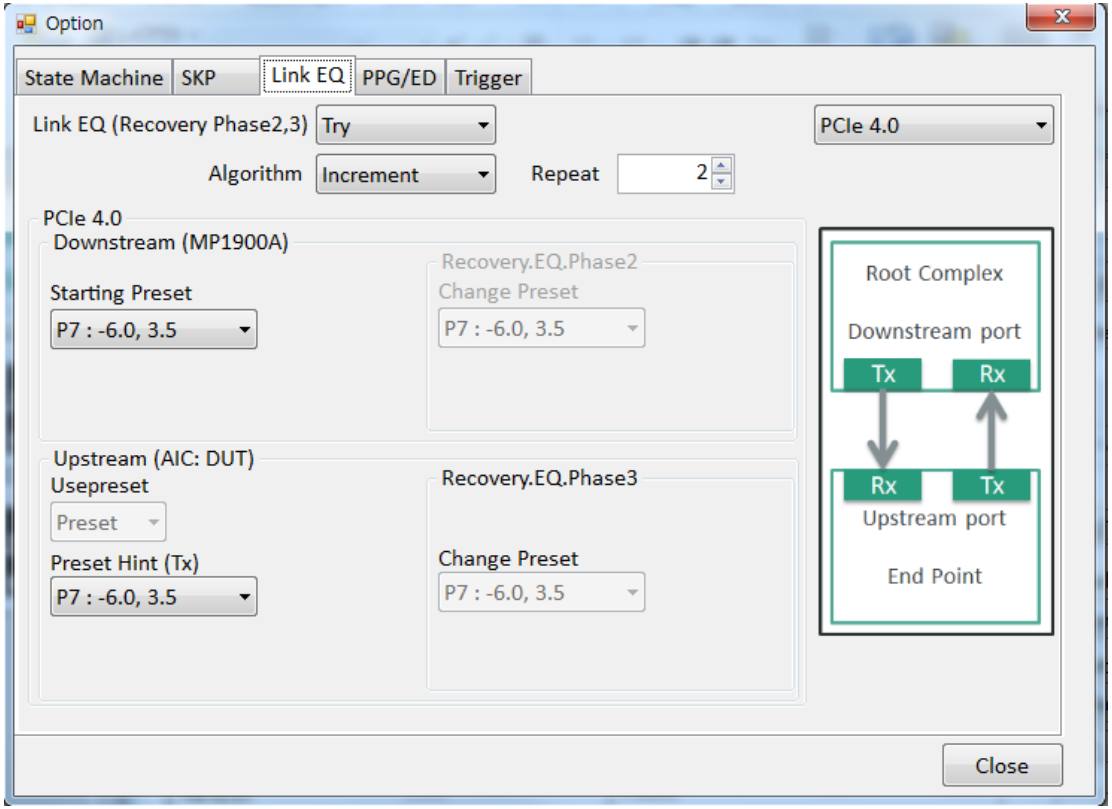


PCIe Link EQ Function

MX183000A
Ver.3.00.00
Added Function

Supports PCIe Gen3 and Gen4 Link EQ Function

- Add-in Card Transmitter Initial TX EQ/Link Equalization Response, and Receiver Link Equalization Tests
- System board Transmitter Link Equalization Response, and Receiver Link Equalization Tests



Appendix

Ordering Information

Model	Name
MP1900A	Signal Quality Analyzer-R
MU181000B	12.5GHz 4port Synthesizer
MU181000B-002	SSC Extension
MU181500B	Jitter Generation Source
MU195020A	21G/32G bit/s PPG
MU195020A-001	32Gbit/s Extension
MU195020A-010	1ch Data Output
MU195020A-020	2ch Data Output
MU195020A-011	1ch 10Tap Emphasis
MU195020A-021	2ch 10Tap Emphasis
MU195020A-030	1ch Data Delay
MU195020A-031	2ch Data Delay
MU195020A-040	1ch Variable ISI
MU195020A-041	2ch Variable ISI
MU195040A	21G/32G bit/s SI ED
MU195040A-001	32Gbit/s Extension
MU195040A-010	1ch ED
MU195040A-020	2ch ED
MU195040A-011	1ch CTLE
MU195040A-021	2ch CTLE
MU195040A-022	Clock Recovery
MU195050A	Noise Generator
MU195050A-001	White Noise

Model	Name
MX183000A-PL001	Jitter Tolerance Test
MX183000A-PL011	PCIe Link Sequence
MX183000A-PL021	PCIe Link Training
MX183000A-PL022	USB Link Training
G0361A	64Gbaud 2-bit DAC with MUX
G0374A	64Gbaud PAM4 DAC
G0375A	32Gbaud Power PAM4 Converter
G0376A	32Gbaud PAM4 Decoder with CTLE
MZ1834A/B	4PAM Converter

*Support for the MU183021A/41B 32G 4ch PPG/ED series will be implemented one-by-one in future. Refer to the MP1900A selection guide for details.

Main Specifications

• Signal Quality Analyzer-R MP1900A

Item	Specification
LCD	12.1" WXGA 1280 x 800
Remote interface	GPIB, LAN
Module slots	8
External equipment interface	USB x6, VGA x1, HDMI x1
OS	Window Embedded Standard 7
Power supply	100 V(ac) to 120 V(ac)/200 V(ac)to 240 V(ac) 50 Hz to 60 Hz
Power consumption	1350 VA max.
Size and mass	340 (W) x 222.5 (H) x 451 (D) mm 20 kg max. (excluding modules)

• 21G/32G bit/s SI ED MU195040A

Item	Specification
Operation bit rate	2.4 Gbit/s to 21 Gbit/s or 32.1 Gbit/s
Number of channels	1 or 2
Input attitude	0.05 Vp-p to 1.0 Vp-p (Single-End) 0.1 Vp-p to 2.0 Vp-p (Differential)
Input sensitivity	15 mV (Eye Height 28.1 Gbit/s)
CTLE	Peak Frequency 14, 8, 4 GHz Gain 0 to –12 dB
Clock Recovery	Yes, supports SSC input
PCIe/USB Link Training	Supported (MX183000A-PL021(PCIe), MX183000A-PL022(USB))
I/O connectors	K (f)

• 21G/32G bit/s SI PPG MU195020A

Item	Specification
Operation bit rate	2.4 Gbit/s to 21 Gbit/s or 32.1 Gbit/s
Number of channels	1 or 2
Output amplitude	0.1 Vp-p to 1.3 Vp-p (Single-end) 0.2 Vp-p to 2.6 Vp-p (Differential)
Emphasis	10Tap
Variable ISI	ISI and Channel Emulation functions
Tr/Tf (20% to 80%)	12 ps (typ.)
Random tutor	115 fs rms (typ.)
PCIe/USB Link Training	Supported (MX183000A-PL021(PCIe), MX183000A-PL022(USB))
I/O connectors	K (f)

• Noise Generator MU195050A

Item	Specification
Number of channels	2
Insertion loss	–3 dB
CMI	0.1 GHz to 1 GHz/1 GHz to 6 GHz
DMI	2 GHz to 10 GHz
White Noise	10 MHz to 10 GHz
Crest Factor	>5

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